Gate-All-Around Nanosheet Transistor for Logic Technology

Maruf Bhuiyan

IBM Research
Outline

- Motivations
- Evolution of Gate-All-Around Transistors
- Nanosheet GAA transistors vs. FINFET

- Nanosheet GAA transistors
  - Process Aspects
  - Device Isolation
  - Multi-Vt Enablement
  - Mobility Considerations

- Conclusions
Microelectronics industry is still powered by scaling by means of device architecture innovations

Fin-FET (tri-gate) faces scaling and performance limitations for future technology nodes

Gate-All-Around devices can unlock further scaling while enhancing performance
Evolution of Gate-All-Around (GAA) Device

- **VLSI 2010**
  - 1st Demo of 300 mm Gate first CMOS Si NW.
  - 1st Demo of Si NW Ring Oscillators.

- **VLSI 2017**
  - 1st Demo of Stacked GAA NS at 7nm ground rules

- **ID/VG**
  - 3 stack devices $L_g=12$nm
  - 44/48nm CPP

- **2008**
  - 1st Demo of Si NW FET at 60nm gate pitch.

- **IEDM 2009**
  - 1st Demo of $L_g$ scaling on Si nanowire (NW)

- **IEDM 2013**
  - 1st Demo of Si NW at 60nm gate pitch.

- **VLSI 2015**
  - 1st Demo of 300 mm RMG CMOS Si NW at 14 nm ground rules.

- **SNMR 2018**
  - Samsung announces Stacked GAA NS for 3nm node.
  - 1st Demo high density SRAM circuit.

- **Decade of R&D on Gate-All-Around (GAA) Architecture.**
- **Device architecture evolved from a single Nanowire to stacked Nanosheet for technology competitiveness.**
Nanosheet device can replace FinFET to enable further technology scaling down beyond 5nm node

This work: Stacked Nanosheet transistor developed at 44/48nm CPP
Single wide nanosheet provides improved $W_{\text{eff}}$ at same footprint over FINFET

N. Loubet et al., VLSI, p. 230-231, 2017
GAA Nanosheet FET vs. FINFET

Relative speed of FinFET vs. GAA Nanosheet FET:

- **Single stack Nanosheet-FET** enables improved frequency performance compared to FinFET or Nanowire-FET

- **Continuously Variable Sheet** enables fine-tuning of power/performance optimization for NS transistors

N. Loubet et al., VLSI, p. 230-231, 2017
GAA Nanosheet FET: Process Aspects

- NS stack epitaxy (a)
- NS “Fin” patterning & STI (b)
- NS “Fin” reveal (c)
- Dummy Gate patterning (d)
- Spacer & Inner Spacer (e)
- Dual SD Epitaxy (f)
- Channel Release (g)
- RMG (h)
- MOL/BEOL (i)
GAA Nanosheet FET: Process Aspects

Stiction of Nanosheet due to surface tension

Optimized IL formation process
Enabling long channel;

P metal residues impact multi-VT enablement

Optimization of etch process

N. Loubet et al., VLSI, p. 230-231, 2017
Gate metal engineering enables multi-VT schemes for GAA NS FET
GAA Nanosheet FET: Device Isolation

- Active Device Isolation is critical for ameliorated short channel effects and off state leakage
- Innovations in the active device isolation enable power/performance gain

J. Zhang et al., IEDM, p. 11.6.4, 2019
GAA Nanosheet FET: Mobility Considerations

- Interplay of different surface orientation determining mobility for GAA NS device
- Variable sheet width provides the flexibility for mobility optimization

C. Yeung et al., IEDM, p. 28.6.1, 2018
GAA Nanosheet FET: Mobility Considerations

- Thickness of silicon sheet influences mobility → interplay between confinement effects and surface orientation

- Interplay between mobility and electrostatics for thinning down sheet thickness

C. Yeung et al., IEDM, p. 28.6.1, 2018
Conclusions

- Nanosheet transistor is demonstrated as a device architecture solution to continue logic scaling post FinFET for technology nodes

- IBM Alliance fabricated and characterized for the first time Horizontally stacked Nanosheet devices with $L_g=12$nm and aggressive 44/48nm CPP

- Stacked GAA Nanosheet has superior electrostatics and enhanced performance compared to scaled FinFETs

- Process innovations related to etching and cleaning critical for successful device fabrication

- Features like full device isolation, multi-VT schemes have been demonstrated
Q/A