Quantum Dot Gate (QDG) SRAMs: Fabrication and Modeling

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Abstract

This paper presents fabrication of quantum dot floating gate non-volatile static random access memory (SRAM). It describes experimental results on quantum dot gate (QDG) inverters that were fabricated in the lab. These inverters exhibited multi-bit operation. Cross-coupled inverters make a SRAM.

A short background of quantum dots assembly in an inverter and forming a static random access memory is described. Energy band diagrams and the equations used to model the device are presented. Then we show you how to create one of these devices using the process files that our group created.

There are many different types of non-volatile memories that have been created, trying to address all of the limitations, but none of them can cover every single one. This is where quantum dots excel. This puts quantum dots at the forefront and gives us a very big reason to pursue research in this field.
Motivation

- Lots of complications with today’s memory
  - Limited storage density
  - Slower speeds as density increases
  - High latency
  - Struggling to keep up with Moore’s Law
- Industry is looking for a financially feasible option
**Background - Quantum Dots based NVMs**

**Quantum Dots:** Quantum dots (QDs) are SiO$_x$-cladded Si nanodots. SiO$_x$ is 0.5-0.75nm and Si core is 4-5nm. They are assembled using a site-specific technique. In the gate region, they form a floating gate sandwiched between two oxide layers called tunnel oxide and control gate oxide. Depending on the gate voltage pulse, channel charge is transferred to quantum dots and determine the state of memory. Multiple bits can be written.

Quantum dot devices offer:

- High storage density
- High durability
- Low operating voltages
Fabricated SRAM photograph

- Pin 1 represents VDD
- Pin 2 represents VSS
- Pin 3 is a two-bit line
- Pin 4 is the gate channel of NMOS transistors
- Pin 5 is connected through the source of the top transistor and the drain of the bottom transistors
Theory Memory Model Equations: Threshold voltage

\[ V_{TH-QDVM} = V_{TH} + \Delta V_{TH} \]

\[ V_{TH} = V_{FB} - \frac{Q_{sc}}{C_{ox}} + 2\psi_B = \left( \phi_m - \frac{Q_{ox}}{C_{ox}} \right) - \frac{Q_{sc}}{C_{ox}} + 2\psi_B \]

\[ \Delta V_{TH} = \frac{Q}{C} = \frac{1}{C_{CG-FG}} \int_{t_w}^{t} j(t) A dt \]

\[ j(t) = q * n_{dot} * N_{QD} * P_{w\rightarrow d} \]

\[ \Delta V_{th} = \frac{Q_{FG}}{C_{CG-FG}} = \left( \frac{1}{C_{CG-FG}} \right) \int_{0}^{t_w} (q * n_{dot} * N_{QD} * P) A dt \]

\[ P_{w\rightarrow d} = \frac{4\pi}{\hbar} \sum_{w,d} \left| \langle \psi_d | H | \psi_w \rangle \right|^2 (f_w - f_d) \delta(E_d - E_w) \]

\[ C_{CG-FG} = \frac{\varepsilon_{CD} \varepsilon_0 A}{d_{CG-FG}} \]
Tunneling rate: from inversion channel to floating Quantum dots

The electrons can tunnel from the inversion channel to a cladded quantum dot in a layer at appropriate VG, the tunneling can be calculated by using the transition rate from QW to QD

\[ P_{W\rightarrow d} = \frac{4\pi}{\hbar} \sum_{W=d} \left| \langle \psi_d \middle| H_t \middle| \psi_W \rangle \right|^2 (f_W - f_d) \delta(E_d - E_W) \]

Schrödinger’s equations

\[ \frac{\hbar^2}{2m} \nabla \left( \frac{1}{m} \nabla \psi_w \right) + (E_n - V) \psi_w = 0 \]

Poisson’s equation

\[ \nabla \cdot (\varepsilon \nabla \phi) = q(n_{QM} + n - N_D^+ - N_A^- - p) \]

Band offsets at the interfaces can be calculated by \( V = q\phi \).

The el distribution (\( n_{QM} \)) in an inversion channel can be calculated

\[ n_{QM} = \sum_n \frac{m^*}{\pi \hbar^2} \Theta(E_F - E_n) \ln \left[ 1 + \exp \left( \frac{E_F - E_n}{kT} \right) \right] |\psi_w|^2 \]
Energy band diagram

<table>
<thead>
<tr>
<th>Layer</th>
<th>Thickness (µm)</th>
<th>$E_g$ (eV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiO$_2$ Floating Gate Oxide</td>
<td>0.0020</td>
<td>9.00</td>
</tr>
<tr>
<td>SiO$_x$ Cladding</td>
<td>0.0010</td>
<td>9.0</td>
</tr>
<tr>
<td>Si QD Core</td>
<td>0.0040</td>
<td>1.12</td>
</tr>
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<td>0.0010</td>
<td>9.0</td>
</tr>
<tr>
<td>SiO$_2$ Gate Oxide</td>
<td>0.0020</td>
<td>9.0</td>
</tr>
<tr>
<td>P-Si Substrate</td>
<td>0.5000</td>
<td>1.12</td>
</tr>
</tbody>
</table>
1. Start with a clean wafer of Silicon
2. Wet-Oxidation (1400 Å)
   a. Place clean wafer inside the wet-oxidation furnace
      i. 4 min at the mouth - 500°C ~ 700°C
      ii. 10 min inside furnace - 1000°C
      iii. 4 min at the mouth - 500°C ~ 700°C
3. Photolithography (S1813)
   a. Apply S1813 Photoresist (Spin at 1000 RPM for 10 sec)
   b. Bake at 115°C for 5 min
   c. Cool for 2 min
   d. Apply Photoresist (Spin at 5000 RPM for 30 sec)
   e. Bake at 115°C for 2 min
   f. Cool for 2 min
   g. Expose with UV light for 18 sec
4. Development and Etching
   a. Bake (1 min)
   b. Cool (1 min)
   c. Prepare Developer (5 parts H2O : 1 Part 351 Developer)
   d. Place wafer in the 351 developer for 10 sec
   e. Place wafer in BOE solution for 140 seconds (etch rate of 10Å per second) to etch the oxide
5. Predeposition
   a. Place wafer in furnace with Phosphorus wafers
      i. 2 min by the opening- 500°C ~ 700°C
      ii. 15 min inside furnace - 1000°C
      iii. 2 min by the opening- 500°C ~ 700°C
Assembling and Annealing Quantum Dots

1. Quantum Dot Solution preparation
   a. Place Si powder along with steel balls in a jar, place jar in a nitrogen box and leave it overnight.
   b. Place jar in the milling machine and perform ball milling for 5 hours.
   c. Place jar in Nitrogen box, scrape finely milled Si powder from the jar.
   d. Add Ethyl Alcohol and Benzoyl Peroxide to Si Powder in appropriate quantities
   e. Sonicate for 3-4 days
   f. Perform Spinning process at 3000, 6000, 9000, 13000, and 13000 RPM for 30 minutes each
   g. Extract clear solution from the vials and prepare QD solution with ethyl alcohol and HF in appropriate amounts for required QD sizes

2. Quantum Dot Self Assembly
   a. Place sample into the QD solution dish for 3 minutes
   b. After 3 minutes have passed, remove the sample and rinse with methanol, blow-dry with Nitrogen
   c. After dried, bring sample to Annealing furnace and place it in there for 5-10 minutes at 750°C
   d. Repeat the quantum dot self-assembly process twice to get four layers of silicon quantum dots (6nm diameter with a 4nm Si core)
1. Dry Oxidation (20 Å)
   a. 2 min at the mouth - 500°C~700°C
   b. 1 min inside furnace - 1000°C (20 Å/min)
   c. 2 min at the mouth - 500°C~700°C
2. Photolithography (S1813)
   a. UV exposure 18 sec
3. Develop for 10 sec
4. Etch (BOE solution 22 sec) to remove 3 layers of dry oxide
5. Aluminum Deposition for metal contact layer
   a. 1500 Angstroms
QDG Inverter - Left QDG - Right FET

- 1500Å Ground contact
- 1500Å Output Voltage contact
- 1500Å Source-Drain Contact
- 1500Å V_{DD} Contact

- 20Å Dry Oxide
- 200Å Dry Oxide
- 4 layers of Silicon QDs
- 1400Å Wet Oxide

*not to scale*
Theoretical vs. Experimental Inverter characteristics

Voltage transfer characteristics

- By having 4 QD layers allow us to have 2 intermediate states.
- As we increase $V_{\text{in}}$, the bottom transistor turns on and the value of $V_{\text{out}}$ decreases. We can see that experimental results follows the ideal trend.
Characteristics of QD gate FET

- The value of drain current will be 0 Amps until V_in value reaches the V_TH value of the device.
- From the last intermediate step, I_D increases until the device is fully opened, thus flat lining, which is what you can see in our experimental data.
Conclusion

- In conclusion, we have presented theoretical model and experimental process steps.
- Inverters were successfully fabricated.
- SRAM data did not work due to misalignment of two cross-coupled inverters.

Bibliography

- F. Jain *ECE 4242 Laboratory Manual*
- Ph.D theses of M. Lingalugari (UCONN 2016)